## REMARKS

With this Response, claims 1-23 are canceled without prejudice. New claims 24-49 are added. Therefore, claims 24-49 are pending.

### OBJECTIONS TO THE SPECIFICATION

The March 10, 2006 Final Office Action ("Office Action") maintains an objection to a header to Table 1, page 8 of the specification. The Office Action quotes the header as reading, "encoded chip sel cts" at states that the meaning of "cts" is unclear. Applicants' file copy of the specification shows the heading as correctly reading "Encoded Chip Selects." Accessing PAIR, Applicants see that the USTPO image of the application has the incorrect "sel ects." The omission of the e in "sel cts" was apparently either a typographical or imaging/copying error. Regardless, Applicants amend the specification to replace "Encoded Chip Sel cts" with "Encoded Chip Selects." The objection is thereby obviated and the correction of this typographical or imaging error is obviously not new matter. Applicants thank the Examiner for pointing out this error in the USPTO image of the application.

### ALLOWABLE SUBJECT MATTER

Applicant appreciates that claims 7 and 19 have been found to have allowable subject matter. The Office objects to these claims because they depend from rejected base claims. However, these claims and the claims from which they depend have been canceled. Therefore, the objection to claims 7 and 19 is moot. Applicant respectfully submits that all of new claims 24-49 are allowable.

### CLAIM REJECTIONS - 35 U.S.C. § 101

The March 10, 2006 Final Office Action, for the first time, rejects claims 20-23 under 35 U.S.C. § 101 as being directed to non-statutory subject matter. That rejection is moot because claims 20-23 are canceled. New claims 47-49 recite a "machine readable physical storage medium." (Emphasis added). To the extent the Office would make the same Section 101 rejection to the new claims 47-49, the rejection is obviated.

**PREMATURE FINALITY OF OFFICE ACTION**

Applicants respectfully traverse the "final" designation of the Final Office Action and request that it be removed. The Final Office Action contains a new ground of rejection – the rejection of claims 20-23 under 35 U.S.C. § 101 as being directed to non-statutory subject matter. The Office Action should not therefore be final. "Under present practice, second or any subsequent actions on the merits shall be final, except where the examiner introduces a new ground of rejection that is [not] necessitated by applicant's amendment of the claims . . . ." MPEP § 706.07(a). Amendments to the claims could not have necessitated this new ground of rejection because rejected claims 20-23 were in their original form.

On June 28, 2006, Michelle Evans, legal assistant to patent attorney Paul A. Mendonsa, spoke by telephone with the Examiner requesting that the finality of the rejection be removed because of the above new ground of rejection. The Examiner would not agree to remove the finality of the rejection without the finality being traversed in a response. The Examiner suggested submitting an amendment and if the amendment overcame the new rejection, the finality would be removed.

Applicants assert that new claims 47-49 are not subject to the above new ground of rejection. However, regardless, Applicants respectfully request that the finality designation be removed in compliance with MPEP § 706.07(a).

Although Applicants are filing a Request for Continued Examination (RCE) with these Amendments/Remarks, if the finality is withdrawn as requested above, Applicants could petition for a refund of the RCE fee. Therefore, Applicants respectfully submit that this request is not mooted by the filing of the accompanying RCE.

**CLAIM REJECTIONS - 35 U.S.C. § 102**

The Office Action rejects claims 1-6, 8-18 and 20-23 under 35 U.S.C. § 102(b) as anticipated by US Patent No. 6,199,151 to Williams et al. (hereinafter "Williams"). All of the above claims have been canceled without prejudice. Therefore, the rejections are moot.

Nevertheless, in order to expedite prosecution, Applicants assert that new claims 24-49 are not anticipated by Williams. The new independent claims recite generating encoded or unencoded chip select words before controller or apparatus configuration, during boot or reset. As an initial matter, these new independent claims do not recite new matter. (See: Specification, Fig. 3 and accompanying text).

Claim 24 reads as follows:

An apparatus comprising:
a controller, to generate, **before controller initialization during boot, reset, or other pre-configuration state of the apparatus**,

an unencoded chip select word in response to a default unencoded chip select mode,
an encoded chip select word in response to a default encoded chip select mode; and
wherein the encoded chip select word and the unencoded chip select word select the same boot device.

(Emphasis added).

Thus, claim 24 recites a controller to generate, **before controller initialization during boot, reset, or other pre-configuration state of the apparatus**, encoded or unencoded chip select

words. Williams does not expressly or inherently teach at least this limitation of claim 24 and therefore does not anticipate claim 24.

Williams does not describe any controller or other device which corresponds to the controller of claim 24. Although Williams appears to describe a row decoder that uses a virtual address translation buffer (Williams, col. 2, lines 43-67), that decoder does not appear to be operable before its configuration, during boot or reset or other pre-configuration state of the system:

> Typically, **each of the device rows in a memory subsystem are mapped** one on top of another such that the top address for one device row is just below the bottom address for another device row. **At startup time, initialization program code (e.g., in a basic input output service (BIOS) device is executed to determine the memory mapping of each of the device rows in the memory subsystem and to program respective top-of-memory values for the device rows into configuration stores in the row decoder 30.** When a physical address is received in the row decoder 30, comparator logic in the row decoder 30 compares the physical address to the top-of-memory values in the configuration registers to generate respective signals indicating whether the physical address is less than (or not less than) the individual top-of-memory values. Using signals generated by comparator logic, elimination logic in the row decoder 30 identifies a device row that is mapped to a region of memory that encompasses the location indicated by the physical address. (Williams, col. 5, lines 40-58) (Emphasis added).

Thus, without the initialization program code that executes at startup time, the Williams row decoder cannot determine where one memory row starts and another begins. The program initialization code configures the Williams row decoder with the memory mappings and top-of-memory addresses that it uses to select device rows. Thus, the Williams row decoder appears to be incapable of generating select words before its configuration, during system startup or reboot. Therefore, Williams does not teach the claimed limitation of a controller that generates chip

select words "before controller initialization during boot, reset, or other pre-configuration state of the apparatus," as recited in claim 24.

In regard to now canceled claim 1, the Office relies on Fig. 2 of Williams as depicting an "address decode" corresponding to the address decoder of claim 1. (Office Action, p. 4). However, nothing in Fig. 2 or in the above-cited portion of Williams indicates that the row decoder would operate before its configuration, during system boot or reset as recited in claim 24.

The office further cites Williams, col. 5 line 55 to col. 6 line 6 and Fig. 3 as describing the address decode as "capable of generate 'unencoded' chip select and 'encoded' chip select." *Id.* This portion of Williams describes a translation look-aside buffer ("TLB 25"). The TLB 25 is described as using row values that are obtained, indirectly through a row value encoder, from the row decoder. (Williams, col. 5, line 58 to col. 6, line 8). The TLB 25 appears dependent upon the row decoder and would therefore be inoperable before the row decoder is configured. Fig. 3 merely shows encoded and unencoded row values, but nothing indicates these row values would be available before the row decoder is configured.

The Office also cites Williams, col. 6, lines 33-50 as describing "TBL hit logic" that "would provides the switching between the encoded and unencoded mode, and the address decoder would provide proper row values in either encoded or unencoded formats . . . ." (Office Action, p. 8). However, as discussed above, it does not appear that the row decoder would be capable of outputting a proper row value before configuration of the row decoder, during boot, reset, or other pre-configuration state of the system, as recited in claim 24.

Thus, the Office does not cite to anything in Williams that teaches at least the above limitation of claim 24. Thus, Williams does not anticipate claim 24.

The remaining independent claims 38, 41, and 47 also recite generating encoded or unencoded chip select words before controller or apparatus configuration, during boot or reset. Based on the above arguments regarding claim 24, they are also not anticipated by Williams. Because dependent claims incorporate all the limitations of the claim from which they depend, dependent claims 25-37, 39-40, 42-46, and 48-49 are also not anticipated by Williams. See: MPEP § 2143.03.

## CONCLUSION

Applicant respectfully requests examination of the above-identified application in view of the present amendment. The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the application.

For at least the foregoing reasons, Applicant submits that the rejections of the claims have been overcome herein, placing all pending claims in condition for allowance. Such action is earnestly solicited. The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the above-identified application.

The Commissioner is authorized to charge or credit any deficiencies or overpayments in connection with this submission to Deposit Account No. 02-2666, and is requested to notify us of same.

Respectfully submitted,
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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail on the below date with sufficient postage in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450

Signature: _____ 8-10-06
Gayle M. Bekish Date